Amendments to the Specification

Please replace the title with the following amended title:

LSI DEVICE HAVING CORE AND INTERFACE REGIONS WITH SOI LAYERS OF DIFFERENT THICKNESS ~~AND MANUFACTURING METHOD OF THE ABOVE~~

Please replace the paragraph beginning on page 4, line 10 with the following amended paragraph:

An LSI device in accordance with a first embodiment includes a high-speed computing portion (a core region) 1 required to operate at low voltage and high speed and a data input/output portion (an interface region or an I/O region) 2, which is a region other than the core region 1 and whose source voltage is high. In the first embodiment, a SOI layer is formed thickly in the I/O region 2 in which the channel length (the gate length) is long while it is formed thinly in the core region 1 in which the channel length is short. Figure 2 is a schematic plan view showing a structure of respective power applying wires in a core region [[14]] 1 and an I/O region [[15]] 2 of a MOSFET device in accordance with a first embodiment. As shown in Figure 2, a [[grand]] ground wiring GND and a core source wiring 1a are provided in the core region 1. In the I/O region 2, provided are a [[grand]] ground wiring GND and an I/O source wiring 2a. Core driving voltage V_{CORE} is applied to the core region 1 through a core source terminal (or a core source circuit) 1b and the core source wiring 1a. I/O driving voltage $V_{I/O}$ is applied to the I/O region 2 through an I/O source terminal (or an I/O

source circuit) 2b and the I/O source wiring 2a. The core driving voltage V_{CORE} is set lower than the I/O driving voltage $V_{I/O}$ in the first embodiment. The core driving voltage V_{CORE} is 1.5 V and the I/O driving voltage $V_{I/O}$ is 3.3 V (or 2.5 V), for example.